Sl No	Particulars		
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3	PhD Thesis Title	"Novel Design and Performance Analysis of High Speed and Low Power Pipeline ADC"	
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7	Brief synopsis The VLSI Technology has evolved so much recently that millions of transistors are integrated on a single chip. Many sub system components are nothing but integrated circuits. The integration of complete electronic system is achieved by combining both analog and digital functions on a single board. CMOS technology plays a key role in mixed signal implementations as it provides high density and low power consumption. The specific implementation such as format conversion, testing interface and layout standards are considered while designing the analog and mixed mode VLSI circuits. Advancement in analog to digital converter technology has achieved high speed, low power consumption and hence low cost in implementation. Some of the good ADC architectures suiting different applications are flash ADC, two-step ADC, pipeline ADC, Successive-Approximation-Register (SAR) ADC, Delta-Sigma ADC, Integrating ADC etc. Among many ADC architectures, the pipeline ADC has the attractive features of maintaining high accuracy at high conversion rate with low complexity and low power consumption. The analog to digital converters play a vital role in today's world of electronic systems. At present, the demand of many is high speed and low power analog to digital converter. The Flash ADC is known for highest conversion rate and low cost and hence used in applications such as wireless communications, digital audio and video systems. The Flash ADC is chosen to work with Pipeline ADC due to high speed and reduced inter-stage delay, which reduces the delay to generate final digital output. In this research work, as Flash ADC is a critical component in pipeline ADC, main focus is given on improvement of Flash ADC. The improvement of Flash ADC improves the performance of pipeline ADC. The Flash ADC mainly depends on comparator and thermometric to binary encoder. Here, the comparator designed has power dissipation in terms of µW. The thermometric to binary encoder is done using full adder logic and multiplexer logic. The results obtained are good and these blocks are used in the construction of 9-bit pipeline ADC. Architecture is designed based on a novel approach of mixed Flash and SAR type and the algorithm is used to design the required sub- ADC block.		